

# **Transformer-Coupled (TC) Technique for the 2:1 Mux and the 1:2 Demux To serialize-and- Deserialize (Serdes) High-Speed Data Sequence**

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**ABSTRACT:** The demand of internet bandwidth is increasing dramatically. The fourth generation Long Term Evolution-Advanced (LTE-A) is developed to increase uplink and downlink mobile communication speeds. The basic backbone optical network must increase data transmission rates to meet public demand. The high speed interface to support the system requirements with energy efficiency is still one of the critical issues. This paper explores the use of transformer-coupled (TC) technique for the 2:1 MUX and the 1:2 DEMUX to serialize-and-deserialize (SerDes) high-speed data sequence. The widely used current-mode logic (CML) designs of latch and multiplexer/demultiplexer (MUX/DEMUX) are replaced by the proposed TC approach to allow the more headroom and to lower the power consumption. The source-offset voltage is decreased so that the supply voltage can be reduced. The lower supply voltage improves the power consumption and facilitates the integration with low voltage supply SerDes interface. The MUX and the DEMUX chips are fabricated in 65-nm standard CMOS process and operate at 0.7-V supply voltage. The chips are measured up to 40-Gb/s with sub-hundred milliwatts power consumption.

**KEYWORDS:** CMOS, Current-mode logic, DEMUX, inductive peaking, latch, MUX, SerDes, transformer coupled technique.

## **I. INTRODUCTION**

The demand for wide-bandwidth networks such as local area networks (LAN), wide area networks(WAN), metropolitan area networks(MAN), very short reach(VSR), storage area networks(SAN) and wireless local area networks(WLAN) is increasing because of the rapid growth of broad band internet access and the performance of computer and storage systems. A wider band width network has also been required in home electronics appliances such as full-motion video, multimedia, e-commerce, and advanced digital services to transfer large-volume image streams. This increase in speed is much higher than the speed increase that corresponds to the famous Moore's law prediction of LSI growth. The way to meet the wide-band width network requirement and then improve performance through low power and low cost is to develop a high-speed CMOS interface and implement it in a system-on-a-chip(SOC).

Today's optical fibre communication systems operate at bitrates between 155-Mb/s and 40-Gb/s. Current high-end communication ICs are mainly implemented

in GaAs, InP, or SiGe bipolar technologies. Several high-speed chips in CMOS technologies are reported, which confirm CMOS to be a viable alternative for high-speed circuit design because advanced circuit techniques and a state-of-the-art fabrication process can be combined to extend speed limits. This approach is very economical due to the lower production costs, higher yield, and integration density. On the other hand, it is desirable to implement low-end chips for 10/100-Mb/s connections at the desk and 1-Gb/s on the LAN back bones using low power CMOS and employing very compact circuit topologies to reduce manufacturing cost.

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## II. RELATED WORK

“Design of 25-Gb/s Half-Rate Clock and Data Recovery Circuit for Optical Communication,” A 25-Gb/s clock and data recovery (CDR) circuit with 1:2 demultiplexer which incorporates a quadrature LC voltage-controlled-oscillator and a half-rate bang-bang phase detector is presented in this paper. A quadrature LC VCO is presented to generate the four-phase output clocks. A half-rate phase detector including four flip-flops samples the 25-Gb/s input data every 20 ps and aligns the data phase. The 25-Gb/s data are retimed and demultiplexed into two 12.5-Gb/s output data. The CDR is designed in TSMC 65nm CMOS Technology. Simulation results show that the recovered clock exhibits a peak-to-peak jitter of 0.524ps and the recovered data exhibits a peak-to-peak jitter of 1.2ps. The CDR circuit consumes 121 mW from a 1.2 V supply.

“A 40Gb/s 14mW CMOS Wireline Receiver,” The proposed receiver uses a “minimalist” approach, which recognizes that every additional stage in the data or clock path consumes more power and limits the bandwidth. The minimalist mentality avoids multiple stages in the front-end continuous-time linear equalizer (CTLE), quadrature oscillators in the clock and data recovery (CDR) circuit, clock or data buffers, or phase interpolation. Moreover, building blocks are shared among different functions so as to reduce the number of current paths between VDD and ground. Using charge-steering techniques extensively, the receiver contains only a few static bias currents adding up to about 6mA. The minimalist approach also leads to a small footprint, about  $110 \times 175 \mu\text{m}^2$ , for the entire receiver, making it possible to design a multi-lane system in a small area and with short interconnects.

“A 40 Gb/s Serial Link Transceiver in 28 nm CMOS Technology,” A 40 Gb/s serial link interface is presented that includes four lanes of transceiver optimized for chip-to-chip communication while compensating for 20 dB of channel loss. Transmit equalization consists of a 2-tap feed-forward equalizer (FFE) while receive equalization includes a 2-tap FFE using a transversal filter, a 3-stage continuous-time linear equalizer with active feedback, and discrete-time equalizers consisting of a 17-tap decision feedback equalizer (DFE) and a 3-tap sampled FFE. The receiver uses quarter-rate double integrate-and-hold sampling. The clock and data recovery (CDR) unit uses a split-path CDR/DFE design which facilitates wider bandwidth and lower jitter simultaneously. A phase detection scheme that filters out edges affected by residual inter-symbol interference allows recovering a low-jitter clock from a partially-equalized eye. A fractional-N PLL is implemented for frequency offset tracking. Combining these techniques, the digital CDR recovers a stable 10 GHz clock from an eye containing 0.8 UIp-p input jitter and achieves 1-10 MHz of tracking bandwidth. The transceiver achieves horizontal and vertical eye openings of 0.27 UI and 120 mV, respectively, at BER =  $10^{-9}$ . The quad SerDes is realized in 28 nm CMOS technology. Amortizing common blocks, it occupies 0.81 mm per lane and achieves 23.2 mW/Gb/s power efficiency at 40 Gb/s.

## III. EXISTING SYSTEM

Current mode logic (CML) is one of the most widely used logic styles for high speed digital circuits. It was initially developed for bipolar transistors, but as MOS technology improved and device-sizes scale down, MOS implementations became practical and attractive (The logic family is sometimes referred to as MOS Current Mode logic or MCML.) In this thesis the terms CML and MCML will be used interchangeably, unless otherwise specified. The general CML circuit consists of three main components (Figure 1): a pull-up load, a pull-down network (PDN) and a constant current source. CML is a completely differential and static logic style and because of this differential nature, it is highly immune to common mode noise. The less than rail-to-rail output swing of a CML device means that the output settling times will be reduced, with the result of faster device operation. It has almost flat power curve over a wide range of frequency as opposed to other logic styles where power consumption increases directly with frequency. At very high frequencies (multi-gigahertz) its power consumption is comparable or even lower than that of other logic styles.

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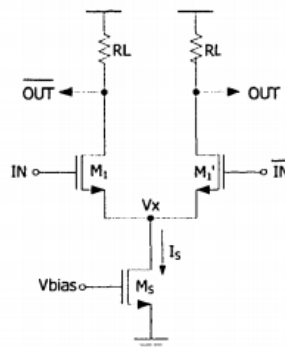


Figure 1: CML Inverter/Buffer.

## The Conventional CML Latch

A conventional current mode logic latch consists of a sample and a hold stage. Current switching between transistor pairs is controlled by complementary clock signals. The sampling pair works as a CML buffer and when it is activated by the clock signal, it tracks the input data and transfers it to the outputs. This is known as the sampling mode of the latch. The hold pair becomes active when the clock polarity changes. The cross-coupled transistors in the hold pair form a regenerative positive feedback structure which retains the output data at the current state.

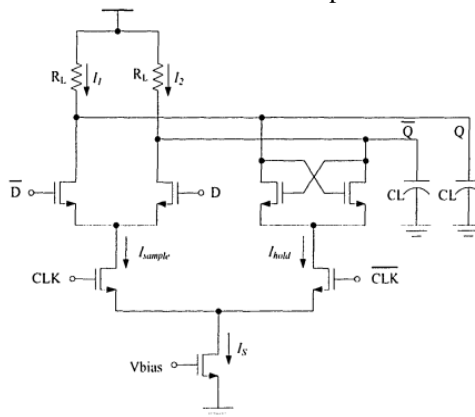


Figure 2: A Conventional current mode logic latch

## IV. PROPOSED SYSTEM

The basic architecture of the SerDes interface is shown in below. In this architecture consists of mainly Mux, PLL and Demux.

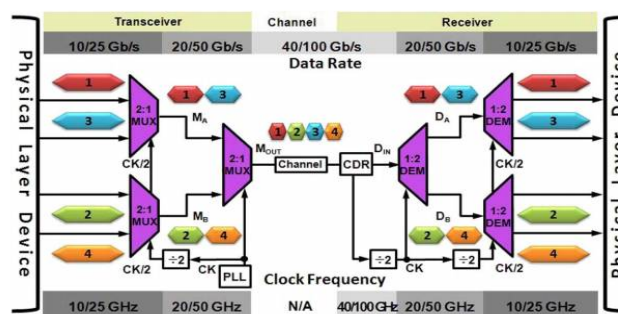


Figure 3: IEEE 802.3ba 40GbE/100GbE backbone SerDes interface.

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Fig. 4 shows transformer-coupled (TC) latch that integrates the TC technique into the CML latch. It consists of the upper-level LVT transistors for two-phase operation and the lower-level secondary winding for two-phase determination. Through the balance transformer, the secondary inductor current  $I_s$  is coupled to the TC latch and selects the drain current from the differential transistor M1-M2 and the cross-coupled transistor M3-M4. Therefore,  $I_{D,M12}$  and  $I_{D,M34}$  are alternatively produced to pull down the differential source voltage,  $V_s = V_{+s} - V_{-s}$ . When CK is logic-high,  $I_s$  flows into the source terminal of M1-M2, and  $V_{+s}$  drops to attract  $I_{D,M12}$  for sensing phase. When CK is logic-low,  $I_s$  flows into the source terminal of M3-M4 instead, and  $I_{D,M34}$  draws for the holding phase. In the 2:1 MUX, the TC latch cooperates with the clock buffer to deliver input clock power and also isolates interference from the other circuits. Thus, the proposed TC latch saves the switching transistors M5-M6 and tail transistor M7 to contribute small flicker noise and allows more headroom for saving supply power.

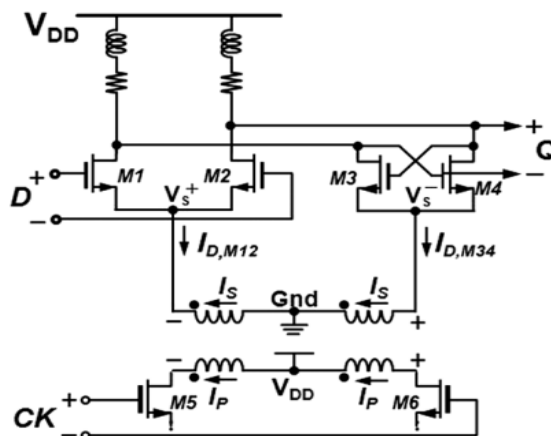


Figure 4: Proposed TC latch with clock buffer.

The SerDes interface consists of the transmitter-end MUX and the receiver-end DEMUX. Fig. 5(a) shows the five-latch architecture of the 1:2 DEMUX that includes two parallel cascading the TC latches with the clock buffer. While the prestage latch L1 delays input data for half of clock cycle,  $CK/2$ , the falling edge triggered retimer recovers the input data for the output D0. Thus, D1 is recovered by the rising edge triggered retimer and aligns with D0. With the mirrored architecture, Fig.5 (b) shows the 2:1 MUX that includes the data-retiming TC latch with the data-combining TC multiplexer core.

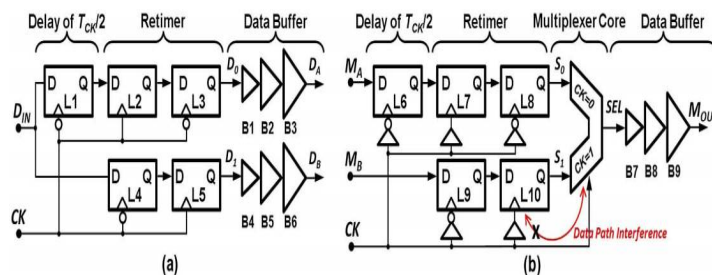


Figure 5: Architecture of (a) 1:2 five-latch DEMUX and (b) 2:1 five-latch MUX.

## TC Latch

Fig. 6 shows the proposed TC latch schematics. A balance-to-unbalance (balun) transformer transfers the single-end clock of CK into the differential source voltage  $V_s$ . In the secondary winding, the equivalent parallel circuit shows the input impedance of  $Z_s = R_s + j\omega L_s$ , where  $L_s$  is the secondary self-inductance and  $R_s$  is the inner series resistor. All NMOS consist of the same size of width-to-length ratio  $W/L$ , of which  $W$  is total channel width and  $L$  is channel length.

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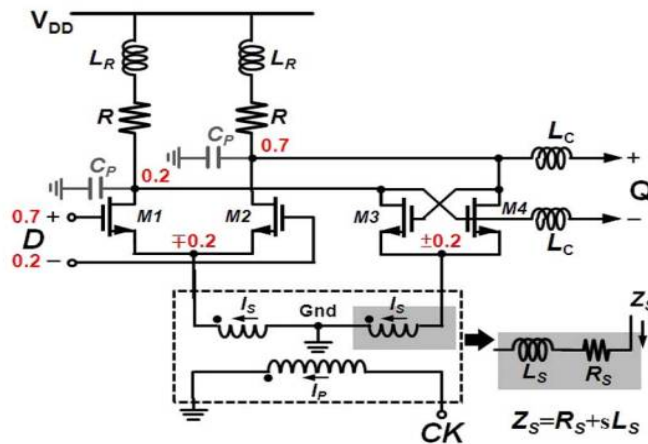


Figure 6: Proposed TC latch in L1-L5.

## TC Latch with Clock Buffer

The 2:1 five-latch MUX adopts the TC multiplexer core and the TC latch to deal with the high data rate. Compared with the 1:2 DEMUX, the isolation between the data path and the clock path is essential. Fig. 7 shows the TC latch cascading down an active clock buffer for isolating the data path interference. To split input clock, the 5-port balun transformer transfers the single-ended CK to the differential input for clock buffer.

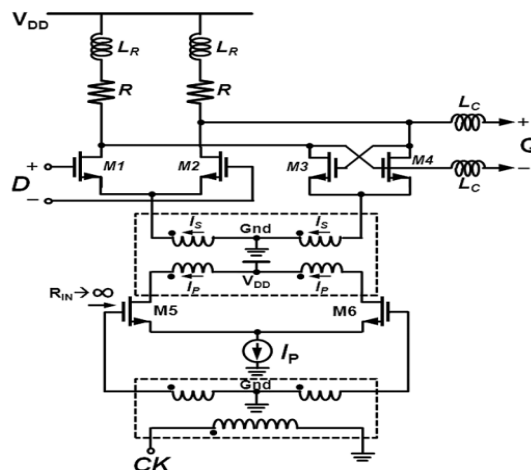


Figure 7: Proposed TC latch with clock buffer in L6-L10.

## TC Multiplexer Core

Fig. 8 shows the modified TC multiplexer core with the single-to-differential balun transformer. Without the isolation transistor, the source offset voltage  $V_s'$  lifts only  $I_s R_s$ , which is lower than the multiplexer core. Therefore, the output swing can be increased even if the reduced supply voltage saves the power consumption. The transformer-coupled current of  $I_s$  directly flows into the M1-M2 and the M3-M4 source terminal to alternate the differential voltage of  $V_s$ .

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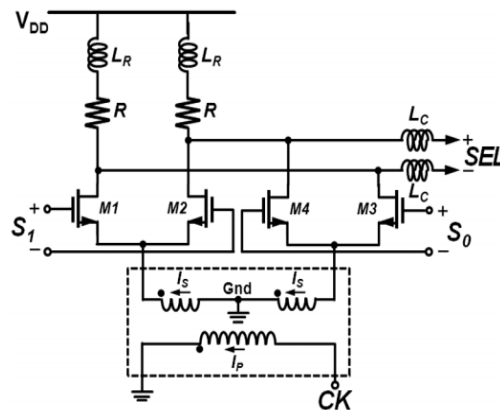


Figure 8: Modified TC multiplexer core with passive balun transformer.

## Data Buffer

Fig. 9 shows the three stages of cascading data buffer. Each stage consists of the differential transistors M1-M6 with the low threshold voltage of  $V_{TH}=0.14V$ . The data buffer amplifies the serialized output of SEL and the deserialized output of D0 and D1. To drive the output 50 ohms load, the fan-out, n, is selected at 1.5 to save the dynamic power in the distributed data buffer.

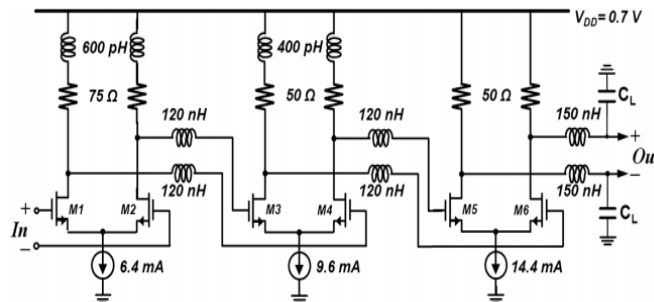


Figure 9: Cascading distributed data buffer.

## V. RESULTS

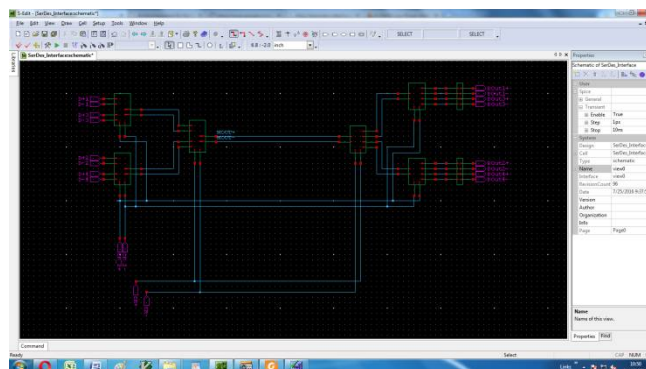


Figure 10: Overall architecture

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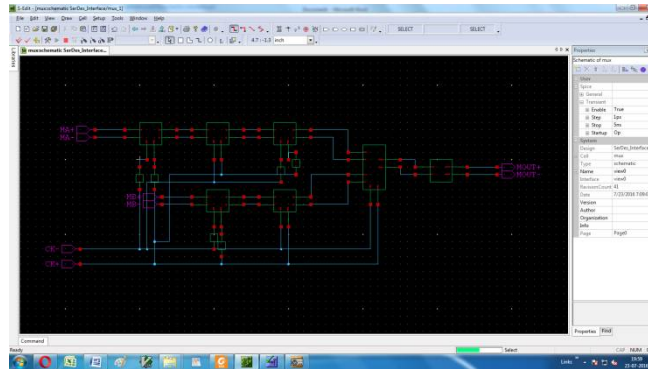


Figure 11: Mux

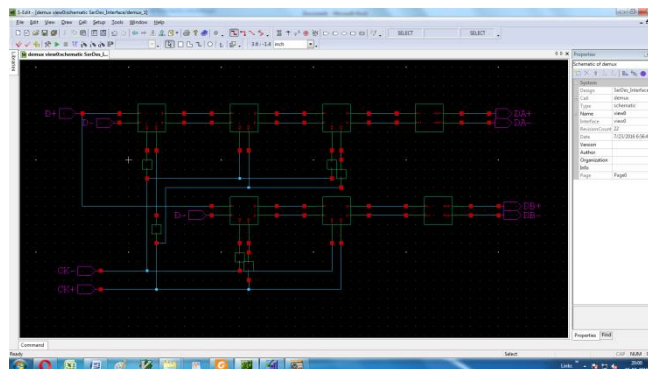


Figure 12: Demux



Figure 13: output

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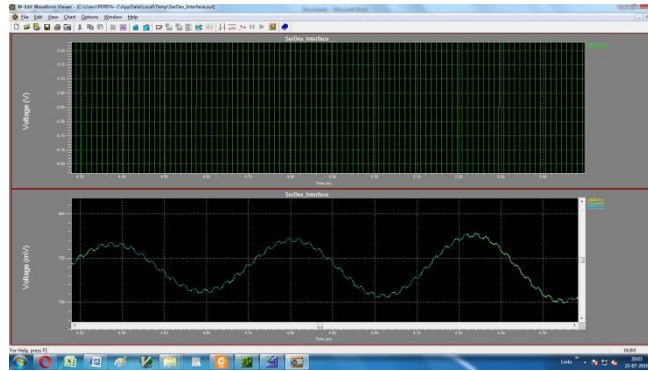


Figure 14: output

## IV. CONCLUSION

In this work, we explore the latch and multiplexer core in SerDes interface based on the Transformer coupled technique for lower power consumption. In the two-phase operation, the transformer-coupled current alternatively pulls down the differential source voltage of the TC designs. The 2:1 MUX and the 1:2 DEMUX chips are fabricated in PMT 45-nm CMOS process to verify the proposed TC based designs. The chips deal with PRBS at the maximum data rate of 40-Gb/s and consume 43.2 milliwatts power at 0.7-V supply voltage

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